Formfactor Specific Hardware Management CMIS-FF Implementation Agreement

OIF-CMIS-FF-01.0

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Implementation Agreement created and approved

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Formfactor Specific Hardware Management (CMIS-FF)

Revision OIF CMIS-FF-01.0

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Abstract:

This Implementation Agreement specifies management control for different modules to provide hardware controls and management in conjunction with CMIS. CMIS-FF in conjunction with CMIS provide an equivalent management to SFF-8472, SFF-8636, and SFP-DD MSA MIS. The function collectively called Formfactor Specific Hardware Management (CMIS-FF).

Table of Contents

1 List of Figures

2 List of Tables

3 Document Revision History

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Table 1: IA Document Revision History

4 Introduction

4.1 Scope

This Implementation Agreement is a supplement to the Common Management Interface Specification [CMIS] to allow control of Form Factor specifics management (CMIS-FF) by defining content of page 05h register map reserved in CMIS for CMIS-FF specifications.

This Implementation Agreement will be referred to as CMIS-FF and is used in conjunction with CMIS [1]. Modules supporting CMIS-FF advertise the capability with Bit 01h:142.3 (see CMIS Table 8-41).

CMIS-FF defines additional management registers to read, control and/or configure optional hardware driven features. The summary of CMIS-FF features are listed below:

- Optional hardware-controlled features implemented
- Registers to control hardware features
- Register to select between hardware or register based control
- Optional digital status of the hardware-controlled signals
- Optional dual purpose hardware control function
- Optional hardware rates select.

The functions associated with the Form Factor Specific Signals defined in this document are already managed using CMIS. Register based status and controls for SFP112, SFP-DD/SFP-DD112, QSFP112, and QSFP-DD/QSFP-DD800 if the equivalent function exists in CMIS then they are not duplicated in the CMIS-FF. Hardware rate selects are required to meet timing of 16 GFC and 32 GFC, see [3], [4]. For speeds beyond 64 GFC [5], such as 128 GFC [6] hardware rate selects are no longer required.

4.2 Required Management Signaling Layer Signals

CMIS-FF is a supplement to CMIS and proper operation of CMIS require following Management Signaling Layer (MSL), see 4.3:

- Reset
- Interrupt
- LowPwrRequestHW

Modules not having the above MSL signals or if a module is configured into an optional mode that one or more of the MSL signal are no longer available will impact operation of CMIS state machines. It is beyond the scope of CMIS-FF how to resolve the operation of CMIS state machine if the module is configured into a mode where one or more of the MSL signals are no longer available.

4.3 Form Factor Specific MSL or MCI Signal Names

Table 2 associates the generic names for management related signals that are used in this specification with 2 form factor-specific signal names, for seven form factor examples. These generic signals form the CMIS Management Signaling Layer (MSL) core (see CMIS section 4.2 and section 5.1) or they are part of a CMIS specified Management Communication Interface (MCI) variant (see CMIS section 4.2 and CMIS Appendix B).

CMIS-FF defines form factor specific extensions to the CMIS MSL core (see CMIS section 2.1.2), while management memory map extensions for the management (advertisement, administration, reporting) of these signals interrupt.

Table 2: Form Factor Dependent Signal Name Associations

CMIS Signal Name	Layer	SFP112	SFP-DD SFP-DD112	QSFP-DD [1]	QSFP2 (QSFP112)	OSFP OSFP-XD	COBO
Reset	MSL	ResetL	ResetL	ResetL	ResetL	RSTn	ResetL
Interrupt		IntL	IntL	IntL	IntL	IntL	IntL
LowPwrRequestHW		NA [2]	LPMode	LPMode	LPMode	LPWn	LPMode
ModSel	I2CMCI	NA	ModSelL	ModSelL	ModSelL	NA	ModSelL

1. QSFP-DD also include QSFP-DD800 and QSFP-DD1600.
2. SFP112 has no dedicate hardware pin for the LPMode signal. As per CMIS 5.3 [2] the module therefore behaves as if the LowPwrRequestHW signal was constantly ASSERTED.

These generic CMIS hardware signals assume two symbolic signal levels, ASSERTED and DEASSERTED (see CMIS section 2.3.2), in order to address realizations both in active-low logic and in active-high logic.

Note per CMIS definition: Active-high voltage signals are sometimes equated, silently, as positive logic bits with a representation of TRUE=1 and FALSE=0, while active-low voltage signals are equated as negative or inverted logic bits, with TRUE=0 and FALSE=1. These silent associations can be confusing and are therefore avoided by introducing symbolic signal levels with a fixed association to the truth values TRUE and FALSE.

The correspondence between the symbolic signal levels ASSERTED and DEASSERTED, and the voltage levels of a given logic convention used in the hardware specification of a form factor is defined in Table 3.

Table 3: Symbolic Logical Signal Values

CMIS Symbolic Value Signal Level	**Active-High Logic** Voltage Level	**Active-Low Logic** Voltage Level	**Positive Bit Logic** CMIS Bool Type	**Boolean Logic** Truth Values
ASSERTED	High	Low	1	TRUE
DEASSERTED	Low	High	0	FALSE

Note per CMIS definition: Boolean logic expressions and equations in CMIS are mostly formulated in terms of numerical bit values 0 and 1, thereby assuming a positive logic representation (TRUE=1 and FALSE=0). Mapping conventions defined in CMIS section 2.3.2 allow the specification to use the abstract signal levels ASSERTED and DEASSERTED for hardware signals together with bit values in those pseudo-Boolean expressions.

4.4 Form Factor Specific versus Generic CMIS Signal Names

Currently form factor specific signals are defined in support of SFP112 [10][15], SFP-DD/SFP-DD112 [9], QSFP112 [13][14], and QSFP-DD/QSFP-DD800/QSFP-DD1600. Table 4 associates generic CMIS/CMIS-FF registers for form factor specific hardware signals. In case of dual mode management control function, the gray signals indicate form factor specific signals that can be selected through CMIS-FF management.

Table 4: Form Factor Dependent Signal Name Association

Function [1] /Names	CMIS Signals	CMIS Registers	SFP2 (SFP112) Signals	SFP-DD/ SFP-DD112 Signals	QSFP2 (QSFP112) Signals	QSFP-DD /QSFP-DD800 /QSFP-DD1600 Signals
Module Reset (control)	Reset	-	ResetL	ResetL	ResetL	ResetL
Interrupt (status)	Interrupt	InterruptDeasserted (00h:03.0)	IntL/TxFault	IntL/TxFaultDD	IntL/RxLOS	IntL/RxLOS
Power mode (control)	LowPwrRequestHW	LowPwrRequestSW (00h:26.4)	NA [2]	LPMode	LPMode/TxDis	LPMode/TxDis
Module select (control)	ModSel		-	-	ModSelL	ModSelL
Per lane Tx Output (control)		OutputDisableTxi <1-2> (10h:130.0-1)		TxDisable TxDisableDD	-	-
Module wide Tx output (control)		TxDisableIsModuleWide (only status: 01h:151.0)	Rsvd/TxDis	TxDisable	LPMode/TxDis	LPMode/TxDis
Per lane Rx_LOS (status)		LOSFlagRxi<1-8> (11h:147.0-1)	NA	RxLOS RxLOSDD	IntL/RxLOS	IntL/RxLOS
Module wide Rx_LOS (status)			Rsvd/RxLOS	RxLOS	IntL/RxLOS	IntL/RxLOS
Per lane Tx failure/ fault (status)		FailureFlagTxi<1-2> (11h:135.0-1)	-	TxFault IntL/TxFaultDD	-	-
Module-wide Tx Failure/Fault (status)		ModuleFault (00h:3:1-3)	-	TxFault	-	-
Tx rates select (control)		ApplyImmediateTxi<1,2> (10h:176.0-1)	-	Speed1 [3] Speed1DD	-	-
Rx rates select (Control)		ApplyImmediateRxi<1,2> (10h:177.0-1)	-	Speed2 [3] Speed2DD	-	-

1. Black in the table indicate default dual mode hardware setting, optional modes are shown in gray and are selected using CMIS-FF registers.

2. SFP112 operates without hardware LPMode signal with LowPwrRequestHW internally asserted forcing the module to boot always in low power.

3. Hardware rate select triggers is a mechanism to trigger CMIS ApplyImmediateTx and ApplyImmediateRx bypassing TWI delay.

Editor Note: OSFP/OSFP-XD and CDFP are not included in the table since we are not aware that these form factor require configurable hardware controls.

4.5 CMIS-FF Module Behavioral Model

Module supporting CMIS-FF follows CMIS [1] Module Behavioral Model in 6.3 with few exceptions described in this section.

4.5.1 Behavior of Hardware Transmit Disable

Hardware TxDis/TxDisable on SFP112, SFP-DD, QSFP112, QSFP-DD/QSFP-DD800/QSFP-DD1600 modules and TxDisableDD on the SFP-DD module interaction with Data Path State Machine (DPSM), CMIS section 6.3.3, makes the following modification to CMIS (Eq. 6-13), where DPDeactivateS (DataPathDeactivateS) transition signals for SFP112, QSFP112, and QSFP-DD/QSFP-DD800/QSFP-DD1600 are defined by the following logic equations, where TxDis controls all module lanes:

DPTxDisableT (SFP112, QSFP112, QSFP-DD) = OutputDisableTx<N>.OR.TxDis (Eq. 4-1)

SFP-DD default mode the TxDisable controls transmit lane 1 and lane 2 of SFP-DD module. DPDeactivateS (DataPathDeactivateS) transition signals for SFP-DD module is defined by the following logic equations, where TxDisable controls both module lanes:

DPTxDisableT (SFP-DD) = OutputDisableTx<N>.OR.TxDisable (Eq. 4-2)

SFP-DD when configured into optional transmit disable mode, see Table 14, the module operates as a dual SFP+ module in one package. In the optional mode DPDeactivateS (DataPathDeactivateS) transition signals for SFP-DD module is defined by the following logic equations, where TxDisable controls lane 1 and TxDisableDD controls lane 2:

DPTxDisableT (SFP-DD) for DP on lane 1= OutputDisableTx<1>.OR.TxDisable (Eq. 4-3)

DPTxDisableT (SFP-DD) for DP on lane 2= OutputDisableTx<2>.OR.TxDisableDD (Eq. 4-4)

Transmit disable is edge triggered, for definition see the SFP-DD and QSFP-DD hardware specifications [7], [8].

4.5.2 Behavior of Hardware Rate Select

SFP-DD module hardware rate selects Speed1, Speed1DD, Speed2, and Speed2DD interaction with CMIS 6.9.3.4 with unidirectional command trigger register in support of FC applications provides fast reconfiguration of the Tx or Rx rates through the hardware controls. Following modification are made to Apply Stage Control Set 0 ApplyImmediateTx and ApplyImmediateRx behavior as defined by the following equations:

ApplyImmediateTx<i> (SFP-DD) = ApplyImmediateTx<1>.OR.Speed1 (Eq. 4-5)

ApplyImmediateTx<2>.OR.Speed1DD (Eq. 4-5)

ApplyImmediateRx<i> (SFP-DD) = ApplyImmediateRx<1>.OR.Speed2 (Eq. 4-6)
ApplyImmediateRx<2>.OR.Speed2DD (Eq. 4-7).

Speed1, Speed2, Speed1DD, and Speed2DD are edge triggered, for definition see the SFP-DD hardware specifications.

4.6 CMIS-FF Management Memory – Page Allocation

The following table lists the pages described in this document. The baseline specification page used to manage form factor specific module is defined in CMIS, [1].

Table 5: CMIS-FF Memory Page Structure

Page Number	Page Name	Page Description
05h	CMIS-FF	Management register in support of SFP112, SFP-DD/SFP-DD112, QSFP112, QSFP-DD/QSFP-DD800/QSFP-DD1600.

4.6.1 Relation to CMIS

CMIS-FF uses terminology mapping, register nomenclature, register names, and register address notation identical to CMIS, see [1].

5 Signal Based Management Features Supported in CMIS-FF

This chapter provides an overview of all CMIS-FF hardware specific functions. This chapter is a summary of Chapter 6 content, but for detail formfactor specific hardware management and the registers please refer to specific sections in Chapter 6:

- SFP112 see *6.1*
- SFP-DD/SFP-DD112 see *6.2*
- QSFP112, QSFP-DD/QSFP-DD800/QSFP-DD1600 see *6.3*.

5.1 IntL/RxLOSL

A dual function hardware pin on QSFP112 and QSFP-DD/QSFP-DD800 modules that optionally can be configured into RxLOSL through CMIS-FF.

RxLOSL is the hardware indicator for loss of signal on any input media lanes and this function is equivalent to CMIS logical OR of LOSFlagRxi<1:8> signals.

5.2 IntL/TxFaultDD

A dual function hardware control on SFP-DD/SFP-DD112 with default set to IntL, optionally through CMIS-FF the hardware function can be configured into TxFaultDD. TxFaultDD indicates transmitter/laser fault on SFP-DD/SFP-DD112 media lane 2. TxFaultDD is equivalent to CMIS FailureFlagTx2 (lane 2).

5.3 LPMode/TxDis

LPMode/TxDis is an optional dual function control on QSFP112 and QSFP-DD/QSFP-DD800 with default set to LPMode. Hardware TxDis is equivalent to CMIS module wide output disable TxDisableIsModuleWide. LPMode is identical to CMIS LowPwrRequest function.

5.4 Hardware Rate Select Control

The SFP-DD MSA [9] defines functional hardware rate select signals for SFP-DD, and SFP-DD112 in support of FC applications. Hardware rates select is required for up to 64 GFC rate FC-PI-7 [5]. FC host transmitters start at fastest capable speed or 32 GFC, then the FC host receiver cycles through speeds supported till both hosts converge to highest supported rate. As the FC hosts go through speed negotiation the FC hosts controls the optical module speed using hardware rate select to change the rate of the optical module quickly without the delay incurred by the TWI. *For speed faster than 64 GFC, such as 128 GFC [6], hardware rate select is not required as FC Link Speed Negotiation (LSN) exchange occurs while the link is operating at 32 GFC.*

Table 6 describes the correlation between hardware based rate select for SFP-DD/SFP-DD112 (in support of FC applications) to CMIS independently controlled Tx and Rx Staged Sets.

For example, hardware rate select Speed1 logic Low (0b) can be utilized to apply ApplyImmediateRx1 (Stage Set 1) and logic High (1b) apply ApplyImmediateRx1 (Stage Set 0).

Host must prepare stage state with datapath initialized.

Module just react to changes to the HW speed select and everting else is host responsibility.

CMIS-FF specification provides the mechanism to use hardware rate selects to control the CMIS Stage Set (0/1) bypassing TWI delay to select between 16 GFC and 32 GFC, see Table 15.

Table 6: Hardware Based and CMIS Rate Selects

Module Type	Lane #	Hardware Rate Select	HW Select State	Conditions	CMIS Equivalent Stage Set
SFP-DD	1	Speed1	Low (0b)	Rx signaling rate of 14.025 GBd (16 GFC)[1]	ApplyImmediateRx1 (Stage Set 1) (controls receive lane 1)
			High (1b)	Rx signaling rate of 28.05 GBd (32 GFC)	ApplyImmediateRx1 (Stage Set 0) (controls transmit lane 1)
		Speed2	Low (0b)	Tx signaling rate of 14.025 GBd (16 GFC)	ApplyImmediateTx1 (Stage Set 1) (controls transmit lane 1)
			High (1b)	Tx signaling rate of 28.05 GBd (32 GFC)	ApplyImmediateTx1 (Stage Set 0) (controls transmit lane 1)
SFP-DD	2	Speed1DD	Low (0b)	Rx signaling rate of 14.025 GBd (16 GFC)	ApplyImmediateRx2 (Stage Set 1) (controls receive lane 2)
			High (1b)	Rx signaling rate of 28.05 GBd (32 GFC)	ApplyImmediateRx2 (Stage Set 0) (controls receive lane 2)
		Speed2DD	Low (0b)	Tx signaling rate of 14.025 GBd (16 GFC) [1]	ApplyImmediateTx2 (Stage Set 1) (controls transmit lane 2)
			High (1b)	Tx signaling rate of 28.05 GBd (32 GFC)	ApplyImmediateTx2 (Stage Set 0) (controls transmit lane 2)

5.4.1 Hardware Based Rate Selection in a CMIS Module

When supported and enabled, hardware rate select signals are mapped in the CMIS module to Unidirectional Data path Reconfiguration (see CMIS, 7.7) to trigger ApplyImmediateTx (see CMIS Table 6-68) and ApplyImediateRx (See CMIS Table 8-73) for faster response to meet FC LSN.

Hardware rate select controls CMIS ApplyImmediate{(Tx1, Tx2, Rx1, and Rx)(Stage Set 0 or 1)} for faster response in support of FC. Prior to engaging hardware rate selects, the host must configure Stage Set Control Set 0 and Stage Set Control 1 through CMIS.

5.5 RxLOS

RxLOS on SFP112 and SFP-DD/SFP-DD112 (media lane 1) is an optional hardware signal equivalent to CMIS LOSFlagRx1.

RxLOS on QFP112 and QSFP-DD/QSFP-DD800 is an optional hardware signal equivalent to CMIS logical "Or"d LOSFlagRx<1:8>.

5.6 RxLOSDD

RxLOSDD on SFP-DD/SFP-DD112 (media lane 2) is an optional hardware signal equivalent to CMIS LOSFlagRx2.

5.7 TxDis(TxDisable)

TxDis(TxDisable)[1] is an optional hardware control on SFP112 to turn off transmitter. Hardware TxDis logical signal is "Or"d with CMIS TxDisableIsModuleWide.

TxDis is an optional hardware control on SFP-DD/SFP-DD112 media lane 1 and is equivalent to CMIS OutputDisableTx1. Optionally TxDisable on SFP-DD/SFP-DD112 can be configured into an equivalent function to CMIS TxDisableIsModuleWide to turn off transmitters on media lane 1 and media lane 2 when they form a common data path. Hardware TxDisable logical signal is "Or"d with CMIS OutputDisableTx1 or TxDisableIsModuleWide depending on the TxDisable mode of operation.

TxDis is an optional hardware control on QSFP112 and QSFP-DD/QSFPDD-800 modules to turn off all transmitters. Hardware TxDis logical signal is "Or"d with CMIS TxDisableIsModuleWide.

5.8 TxDisableDD

TxDisableDD is an optional control on SFP-DD/SFP-DD112 media lane 2 and is equivalent to CMIS OutputDisableTx2. Hardware TxDisableDD logical signal is "Or"d with CMIS OutputDisableTx2 to turn off transmitter on media lane 2.

5.9 TxFault

TxFault is a hardware control on SFP-DD/SFP-DD112 module and by default indicates module wide fault. The function of TxFault is equivalent to CMIS logical OR of FailureFlagTx1 and FailureFlagTx2.

[1] Hardware TxDis and TxDisable have identical functions. SFP112, QSFP112, QSFP-DD/QSFP-DD800 hardware disable function is called TxDis, but SFP-DD/SFP-DD112 calls the same function TxDisable.

Optionally TxFault on SFP-DD/SFP-DD112 modules can be configured to indicate fault on transmit media lane 1 only.

6 Form Factors Currently Utilizing CMIS-FF

Current version of CMIS-FF provides hardware management support for following module form factors:

- SFP112
- SFP-DD/SFP-DD112
- QSFP112 and QSFP-DD/QSFP-DD800/QSFP-DD1600.

For detail of SFP112 hardware specifications, see [10], [15]. For detail of QSFP112 hardware specifications, see [13], [14]. For detail of SFP-DD/SFP-DD112 hardware specifications, see [9]. For detail of QSFP-DD/QSFP-DD800/QSFP-DD1600 hardware specifications, see [8].

6.1 CMIS-FF Support for SFP112

CMIS provides the base management of SFP112, but some of the optional SFP112 features are management through CMIS-FF. The SFP112 features that must managed with CMIS-FF are listed in this section.

CMIS specifications [1] with addition of CMIS-FF specifications provide an equivalent management to support SFP112 similar to SFF-8472 [11] but with addition of hardware ResetL and optional LPMode.

6.1.1 Optional TxDis

TxDis is an optional hardware control function on SFP112. CMIS-FF allows masking the hardware TxDisable signal, a register indicating TxDis hardware implemented, and a register to indicating digital status of hardware TxDisable. Hardware TxDis logical signal is “Or”d with CMIS TxDisableIsModuleWide.

TxDis register advertisement and controls are defined in the CMIS-FF, see page 05h Table 11 and Table 14.

6.1.2 Optional RxLOS

RxLOS is an optional hardware loss of signal indicator on SFP112. CMIS-FF provides status register if optional RxLOS hardware control is implemented, a register to select and enable the optional RxLOS. RxLOS is an optional hardware signal equivalent to CMIS LOSFlagRx1.

RxLOS is advertised and controlled in the CMIS-FF, see page 05h Table 11 and Table 12.

6.2 CMIS-FF Support for SFP-DD/SFP-DD112

CMIS provides the base management for SFP-DD/SFP-DD112, but the form factor specific hardware features of SFP-DD/SFP-DD112 are management with CMIS-FF. The SFP-DD/SFP-DD112 features that must managed with CMIS-FF are listed in this section.

CMIS specifications [1] with addition of CMIS-FF specifications provide an equivalent management similar to the SFP-DD MIS [7][11] to support SFP-DD/SFP-DD112.

6.2.1 TxDisable

TxDisable is a hardware control function on SFP-DD/SFP-DD112. CMIS-FF allow masking the hardware TxDisable signal, a register indicating hardware implementation of TxDisable, and digital status of hardware TxDisable control.

TxDisable is equivalent to CMIS OutputDisableTx1. Optionally TxDisable on SFP-DD/SFP-DD112 can be configured into an equivalent function to CMIS TxDisableModuleWide to turn off transmitters on media lane 1 and media lane 2 when they form a common data path. Hardware TxDisable logical signal is "Or"d with CMIS OutputDisableTx1 or TxDisableIsModuleWide depending on the TxDisable mode of operation.

TxDisable is advertised and controlled in the CMIS-FF, see page 05h Table 11 and Table 14.

6.2.2 TxDisableDD

TxDisableDD is a hardware control function on SFP-DD/SFP-DD112. CMIS-FF allows masking the hardware TxDisable signal, a register indicating hardware implementation of TxDisableDD, and digital status of hardware TxDisable control.

TxDisableDD is equivalent to CMIS OutputDisableTx2. Hardware TxDisableDD logical signal is "Or"d with CMIS OutputDisableTx2.

TxDisableDD is advertised and controlled in the CMIS-FF, see page 05h Table 11 and Table 14.

6.2.3 RxLOS

RxLOS is a hardware indicator signal on SFP-DD/SFP-DD112. CMIS-FF provides status register if optional RxLOS hardware control is implemented, a register to configure RxLOS to indicate loss of signal on media lane 1 or media lane 1 and 2. RxLOS is an optional hardware signal is equivalent to CMIS LOSFlagRx1 when RxLOS is an indicator of media lane 1, when RxLOS is configured to be module wide (lanes 1 and 2) the hardware signal is equivalent to CMIS LOSFlagRx1 "Or"d LOSFlagRx2.

RxLOS advertised and controlled in the CMIS-FF, see page 05h Table 11 and Table 12.

6.2.4 RxLOSDD

RxLOSDD is a hardware indicator signal on SFP-DD/SFP-DD112 media lane 2. CMIS-FF provides status register if optional RxLOSDD hardware control is implemented. RxLOSDD is an optional hardware signal is equivalent to CMIS LOSFlagRx2.

It is advertised and controlled in the CMIS-FF, see page 05h Table 11 and Table 12.

6.2.5 TxFault

TxFault is a hardware signal on SFP-DD/SFP-DD112 indicating fault on media lane 1. The function of TxFault is equivalent to CMIS FailureFlagTx1 (lane 1) when SFP-DD is configured as a dual SFP, when SFP-

DD is configured into a two lanes module then TxFault become equivalent of CMIS FailureFlagTx1 “Or”d FailureFlagTx2.

Support of optional TxFault is advertised in the CMIS-FF, see page 05h Table 13.

6.2.6 IntL/TxFaultDD

TxFault/IntL Dual function hardware control on SFP-DD/SFP-DD112 with default set to IntL. Optionally through CMIS-FF the hardware function can be configured into TxFaultDD signal indicating fault on media lane 2. TxFaultDD is equivalent to CMIS FailureFlagTx2 (lane 2).

IntL and TxFaultDD are advertised and controlled in the CMIS-FF, see page 05h Table 13.

6.2.7 Speed1 and Speed2

Speed1 and Speed2 are hardware rate select controls on the SFP-DD/SFP-DD112 controlling transmit and receive lane 1, see Table 6.

Speed1 and Speed2 are advertised and controlled in the CMIS-FF, see page 05h Table 15.

6.2.8 Speed1DD and Speed2DD

Speed1DD and Speed2DD are hardware rate select controls on the SFP-DD/SFP-DD112 controlling transmit and receive lane 2, see Table 6.

Speed1DD and Speed2DD are advertised and controlled in the CMIS-FF, see page 05h Table 15.

6.3 CMIS-FF Support for QSFP112 and QSFP-DD/QSFP-DD800/QSFP-DD1600

CMIS provides the base management for QSFP112 and QSFP-DD/QSFP-DD800/QSFP-DD1600, but some of the optional QSFP-DD/QSFP-DD800 features are management through CMIS-FF. The QSFP112 and QSFP-DD/QSFP-DD800 features that are managed with CMIS-FF are listed in this section.

CMIS specifications [1] with addition of CMIS-FF specifications provide an alternative to management support of QSFP112/QSFP-DD/QSFP-DD800/QSFP-DD1600 by SFF-8636 [12][11].

6.3.1 LPMode/TxDis

LPMode/TxDis is an optional dual function control pin on QSFP112 and QSFP-DD/QSFP-DD800/QSFP-DD1600 with default set to LPMode. Hardware TxDis is equivalent to CMIS module wide output disable TxDisableIsModuleWide.

Optional support of TxDis is advertised and controlled in the CMIS-FF, see page 05h Table 10 and Table 14.

6.3.2 IntL/RxLOSL

IntL/RxLOSL is an optional dual function control pin on QSFP112 and QSFP-DD/QSFP-DD800/QSFP-DD1600 modules with default set to IntL. RxLOSL is the hardware indicator for loss of signal on any input media lanes and this function is equivalent to CMIS logical OR of LOSFlagRxi<1:8> signals.

Support of optional RxLOSL is advertised and controlled in the CMIS-FF, see page 05h Table 10 and Table 12.

6.4 CMIS-FF Module Active Firmware Version

The Bytes described in Table 16 allow a module to report the firmware major and minor revision for the active CMIS-FF (i.e., currently running) firmware, or to indicate that no firmware is running.

Note: Module firmware may consist of multiple firmware components (program images, non-volatile data). It is strongly recommended that the firmware version identifies the aggregate (or bundle) of all firmware element that can be updated by the vendor or by the host.

Note: For modules supporting firmware update, it is also strongly recommended that the firmware major and minor revision numbers together with build number uniquely specifies exactly one aggregate firmware configuration. Firmware aggregates that differ in only a single component should never have the same version identification (major, minor, build).

Note: The identification of temporary firmware component versions for lab test or debug, or identification of individual firmware components is not in the scope of this specification.

Reporting firmware version information is generally required and independent of whether a module supports firmware update by any method. Content and meaning of firmware major and minor revision information reported are vendor dependent, but the format of both fields is defined to be integer. The encoding of the major and minor revision fields is:

- Major Revision = 0 and Minor Revision = 0 indicates that a module does not have any firmware.
- Major Revision = FFh and Minor Revision = FFh indicates that the active firmware image is invalid.
- All other Major and Minor Revision combinations indicate the active firmware version.

Note: Flat memory modules with firmware may also report their active firmware version in these Bytes.

Note: Modules that support a proprietary vendor specific firmware update method (instead of CDB as described later) shall still report the active firmware version in these bytes.

6.5 CMIS-FF Custom

Custom CMIS-FF register fields Table 17 are under control of each individual module vendor. The same custom resource may be used differently by different vendors or groups of vendors.

7 Module Management Memory Map

This chapter defines the structure and the meaning of the registers and fields in the Management Memory Map of a CMIS-FF compliant module.

Some items are repeated from CMIS for reader's convenience. In case of discrepancy the CMIS definition will have precedence.

7.1 Overview and General Specifications

CMIS-FF uses register access protocol defined in CMIS section 5.2. CMIS has allocated page 05h for CMIS-FF usage, see Figure 1. CMIS-FF defines content of page 05h register for management of form factor specific hardware and functions.

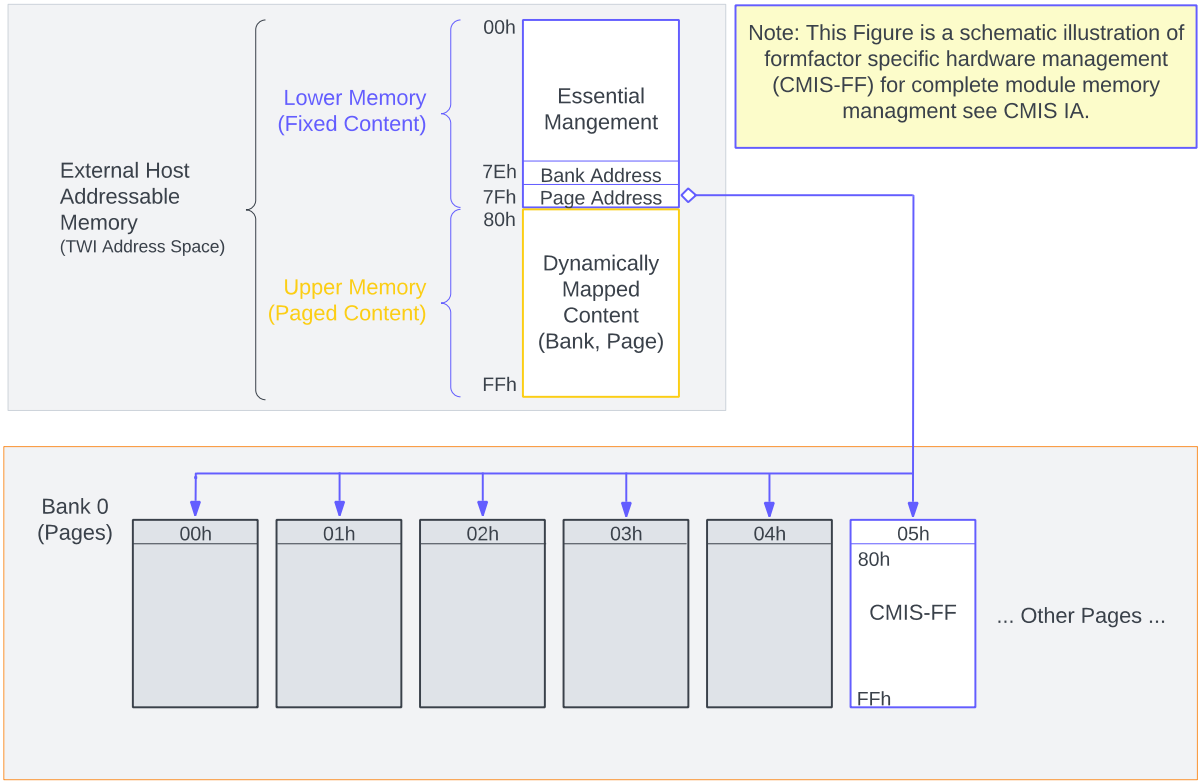

Figure 1: CMIS-FF Module Memory Map (Conceptual View)

7.2 Register Default Values

Default values for all control registers are 0 unless otherwise specified.

Note: Hosts are encouraged to review or explicitly set critical registers and not rely on module default values.

The default value of Masks for Flags residing on optional pages is 1 (Interrupt is masked by default).

Note: A default value of 1 is also recommended for all Masks of custom Interrupt sources.

7.3 Byte Order

The default byte order of multi-byte registers representing numerical types is big endian, i.e., the lowest byte address contains the most significant byte of the multi-byte value. Exceptions are stated explicitly.

Note: Independent of proper representation, atomic accesses to multi-byte registers may require access synchronization protocols (see also CMIS section 5.2.3 for a discussion of data coherency).

7.4 Access Type

The following Field access types Table 7 are distinguished and indicated (together with an optionality indication) in the Type column of the field definition tables defining the Management Memory Map later in this chapter. The word "element" is used here to refer to an entire Byte, a Field, or a Bit. For additional detail see CMIS 8.1.3.6.

Table 7: Access Types

Access Type	Description
RW	A **readable** and **writeable** element.
RWW	A **readable** and **writeable** element that can also be **modified** by the module. Note: This access type should be used only for interactions governed by a protocol.
RO	A **read-only** element. A WRITE of a value to a read-only element is allowed but has no effect.
WO	A **write-only** element. A READ from a write-only element is **allowed** but delivers **unpredictable** values.
WO/SC	A **write-only** element with **self-clearing** side effect. A READ from a WO/SC element is **allowed** and delivers a **zero** value, except transiently when reading before the module has evaluated and cleared the non-zero bits written.
RO/COR	A **read-only** element with **clear-on-read** (clear-after-read) side effect. All bits in a RO/COR Byte are cleared by the module after the Byte value has been read. Note: Modules may also combine clearing and update (clear-or-update-on-read).

7.5 Optionality Indications

Identified elements of the Memory Map described in this chapter are conditionally or unconditionally optional. For additional detail see CMIS 8.1.3.7. An optional element is either supported or not supported by a specific module, see Table 8.

Table 8: Optionality Indications

Access Type	Abbreviation	Description
Required	**Rqd.**	always supported when the relevant Page is supported
Advertised	**Adv.**	supported when indicated in a clearly associated feature advertisement
Conditional	**Cnd.**	supported when some (documented) run-time evaluated condition is present
Optional	**Opt.**	optionally supported, unknown conditions, inferred only from feature behavior

7.6 Page Mapping (Upper Memory Content Selection)

The **PageMapping** register (00h:126-127) is a **two-byte** register containing a **Page Address** value that determines which register in the internal Management Memory Map is **actually** accessed when the host performs an ACCESS addressing a Byte in Upper Memory (Byte address range 128-255), see CMIS 8.2.13.

Note: This programmable redirection from a fixed Upper Memory address window to a selected Page in the Management Memory Map is referred to as Page Mapping. Note that CMIS-FF is agnostic of how a module actually implements or emulates page mapping.

7.7 Page 05h (CMIS-FF)

Page 05h is an optional Page containing advertising and control fields for properties of paged memory modules. The module advertises support of Page 05h in the MemoryModel Bit 01h:142.3.

Support for CMIS-FF is advertised in the base CMIS Table 8-46 [1], and relevant CMIS hardware related registers are highlighted below:

- Hardware RxLOS on SFP112 and hardware RxLOS/RxLOSDD on SFP-DD/SFP-DD112 are equivalent to per lane CMIS LOSFlagRx<i>, see page 11h Byte 147.
- Hardware TXFault/TxFaultDD on SFP-DD/SFP-DD112 is equivalent to CMIS per lane FailureFlagTx<i>, page 11h Byte 135.
- Hardware TxDis on SFP112 and hardware TxDisable/TxDisableDD on SFP-DD/SFP-DD112 are equivalent to CMIS per lane output disables, see OutputDisableTx<i> page 10h Byte 130.
- Hardware TxDis on QSFP112 and QSFP-DD/QSFP-DD800/QSFP-DD1600 is equivalent to CMIS module wide output disable, see TxDisableIsModuleWide page 01h:151.0.

Table 9 is an overview of the CMIS-FF page providing management status and controls for SFP112, SFP-DD/SFP-DD112, QSFP112, and QSFP-DD/QSFP-DD800/QSFP-DD1600.

Table 9: Page 05h CMIS-FF Overview

Byte	**Size** (bytes)	**Description**
128	1	Dual mode management status reporting, see Table 10
129	1	Dual mode management control, Table 11
130	1	Module RxLOS Status, Table 12
131	1	TxFault Status and control, Table 13
132	1	TxDisable Status and Control, Table 14
133	2	FC Rate Select, Table 15
134-254	121	**Reserved [121]**
255	1	Page Checksum of bytes 128-254

Table 10: Page 05h Dual Mode Hardware Support Advertising

Byte	Bit	Name	Field Description	Type
128	7	TxFaultModeSupported	SFP-DD/SFP-DD112 TxFault hardware is supported 0b: No 1b: Yes	Adv. RO
	6	TxFaultDDModeSupported	SFP-DD/SFP-DD112 TxFaultDD hardware is supported 0b: No 1b: Yes	Adv. RO
	5	RxLOSLModeSupported	SFP112, QSFP112, QSFP-DD/QSFP-DD800 RxLOSL is hardware supported 0b: No 1b: Yes	Adv. RO
	4-0		**Reserved**	

Table 11: Page 05h Dual Mode Hardware Pin Control

Byte	Bit	Name	Field Description	Type
129	7		**Reserved**	Adv. WO
	6	SelectTxDisable	On SFP112 module select optional TxDis 0b: Rsvd 1b: TxDis	Adv. RW
	5	SelectRxLOSL	On SFP112 module select optional RxLOSL 0b: Rsvd 1b: RxLOSL Mode	Adv. RW
	4	SelectTxFaultDD	On SFP-DD/SFP-DD112 modules change the default IntL to TxFault 0b: IntL 1b: TxFault	Adv. WO
	3	SelectTxDisableQ	On QSFP112, QSFP-DD/QSFP-DD800 change the default LPMode to optional TxDis 0b: LPMode 1b: TxDis	Adv. RW
	2	SelectRxLOSLQ	On QSFP112, QSFP-DD/QSFP-DD800 change the default IntL Mode to optional RxLOSL 0b: IntL Mode 1b: RxLOSL Mode	Adv. RW
	1-0		**Reserved**	

Table 12: Page 05h SFP-DD Module RxLOS Advertisement and Control

Byte	Bit	Name	Field Description	Type
130	7	HWRxLOSSupported	Hardware RxLOS implemented on SFP-DD/SFP-DD112 for media lane 1 0b: HW RxLOS not implemented 1b: HW RxLOS implemented	Adv. RO
	6	HWRxLOSDDSupported	Hardware RXLOSDD implemented on SFP-DD/SFP-DD112 for media lane 2 0b: HW RxLOSDD not implemented 1b: HW RxLOSDD implemented	Adv. RO
	5	HWRxLOSModuleWide	Hardware RxLOS on SFP-DD/SFP-DD112 configured module wide 0b: LOS is per lane 1b: Configured module wide	Adv. RW
	4-0		**Reserved**	RO

Table 13: Page 05h SFP-DD Hardware TxFault Advertisement and Controls

Byte	Bit	Name	Field Description	Type
131	7	HWTXFaultSupported	Hardware TXFault implemented on SFP-DD/SFP-DD112 on media lane 1 0b: No 1b: Yes	Adv. RO
	6	HWTXFaultDDSupported	Hardware TXFaultDD implemented on SFP-DD/SFP-DD112 media lane 2 0b: No 1b: Yes	Adv. RO
	5	HWTxFaultMode	Configure TXFault for SFP-DD/SFP-DD112 to be module wide (media lane 1 and 2) 0b: Module wide 1b: Media Lane 1	RW
	4-0		**Reserved**	

Table 14: Page 05h Hardware TxDisable Advertisement and Controls

Byte	Bit	Name	Field Description	Type
132	7	HWTXDisableSupported	Hardware TxDis/TxDisable implemented on SFP112, SFP-DD/SFP-DD112 media lane 1, QSFP112, and QSFP-DD/QSFP-DD800/QSFP-DD1600 modules 0b: HW TxDis not implemented 1b: HW TxDis implemented	Adv. RO
	6	HWTXDisableDDSupported	Hardware TXDisableDD implemented on SFP-DD/SFP-DD112 media lane 2 0b: HW TxDisableDD not implemented 1b: HW TxDisableDD implemented	Adv. RO
	5	DigitalStatusTxDisable	Register indicating digital status of TxDisable hardware signal on SFP112, SFP-DD/SFP-DD112 lane 1, QSFP112, QSFP-DD/QSFP-DD800/QSFP-DD1600 0b: Transmitter is on 1b: Transmitter is turned off	Adv. RO
	4	DigitalStatusTxDisableDD	Register indicating digital status of TxDisableDD hardware signal on SFP-DD/SFP-DD112 lane 2 0b: Transmitter is on 1b: Transmitter is turned off	Adv. RO
	3	MaskHWTxDisable	Register masking hardware TxDisable to allow controlling media lanes solely through CMIS OutputDisable1 0b: Media lane 1 controlled by “OR”d TxDisable and CMIS OutputDisable1 (in case TxDisable configured into module wide mode on SFP-DD/SFP-DD112 then media lane 1 and 2 are controlled by the “OR”d TxDisable and TxDisableIsModuleWide) 1b: Media Lane 1 controlled only by CMIS OutputDisable1	Adv. RW
	2	MaskHWTxDisableDD	Register masking hardware TxDisableDD to allow controlling media lanes solely through CMIS OutputDisable2 0b: Media lane 2 controlled by “OR”d TxDisable and CMIS OutputDisable1 1b: Media Lane 1 controlled only by CMIS OutputDisable1	Adv. RW
	1	TxDisableModes	Register configuring TxDisable mode of operation on SFP-DD/SFP-DD112 0b: TxDisable is module wide and controls media lane 1 and 2 that form a data path, in such cases TxDisableDD is ignored. 1b: TxDisable controls media lane 1 and TxDisableDD controls lane2.	Adv. RW
	0		**Reserved**	

Table 15: Page 05h Fibre Channel Rate Select

Byte	Bit	Name	Field Description	Type
133	7	HWRateSelectSupported	Module supports hardware rate select 0b: Not supported 1b: Supported	Adv. RO
	6	RateSelectMode	Rate selection by HW signals 0b: Enabled. The state of the rate select hardware signal(s) determines which preprogrammed CMIS staged control set is applied during configuration (ApplyDPInit) or applied on state change of these signals (ApplyImmediate). 1b: Disabled. The rate selection hardware signals are not evaluated. The module behaves like a regular CMIS module.	Adv. RO
	5-0		**Reserved**	
134	7	HWStatusSpeed1	Logical status of SFP-DD/SFP-DD112 lane 1 receive CDR rate 0b: 16 GFC 1b: 32 GFC	Adv. RO
	6	HWStatusSpeed2	Logical status of SFP-DD/SFP-DD112 lane 1 transmit CDR rate 0b: 16 GFC 1b: 32 GFC	Adv. RO
	5	HWStatus1DD	Logical status of SFP-DD/SFP-DD112 lane 2 receive CDR rate 0b: 16 GFC 1b: 32 GFC	Adv. RO
	4	HWStatusSpeed2DD	Logical status of SFP-DD/SFP-DD112 lane 2 transmit CDR rate 0b: 16 GFC 1b: 32 GFC	Adv. RO
	3-0		**Reserved**	

Table 16: Page 05h CMIS-FF Module Firmware Version

Byte	Bit	Name	Field Description	Type
135	7-0	CMISFFActiveFirmwareMajorRevision	U8 Numeric representation of the module's RO active firmware major revision	RO Rqd.
136	7-0	CMISFFActiveFirmwareMinorRevision	U8 Numeric representation of the module's RO active firmware minor revision	RO Rqd.

Table 17: Page 05h CMIS-FF Custom Pages

Byte	Bit	Name	Field Description	Type
245-255	7-0	Custom	Reserved for custom use	RW

8 References

8.1 Normative references

[1] Common Management Interface Specification (CMIS) 5.2, see https://www.oiforum.com/wp-content/uploads/OIF-CMIS-05.2.pdf .
[2] Common Management Interface Specification (CMIS) 5.3 editor draft, see https://www.oiforum.com/bin/c5i?mid=4&rid=5&gid=0&k1=54108.

8.2 Informative references

The following interface standards and specifications are relevant to this Specification.

[3] ANSI FC-PI-5 16GFC (INCITS 479)
[4] ANSI FC-PI-6 32GFC (INCITS 533)
[5] ANSI FC-PI-7 64GFC (INCITS 543)
[6] ANSI FC-PI-8 128GFC (INCITS 560)
[7] SFP-DD Management Interface, Rev. 2.0, http://sfp-dd.com/specification/
[8] QSFP-DD/QSFP-DD800/QSFP112 Hardware Specification for, QSFP DOUBLE DENSITY 8X AND QSFP 4X PLUGGABLE TRANSCEIVERS, Revision 7.0, http://www.qsfp-dd.com/specification/
[9] SFP-DD/SFP-DD112/SFP112 Hardware Specification for SFP Double Density Pluggable Transceiver, Revision 5.2, http://sfp-dd.com/specification/
[10] SFF-8419 SFP+ Power and Low Speed Interface, Rev. 1.3
[11] SFF-8472 Diagnostic Monitoring Interface for Optical Transceivers, Rev. 12.4.
[12] SFF-8636 Management Interface for Cabled Environments, Rev. 2.11
[13] SFF-8679 QSFP28 4X Base Electrical Specifications, Rev. 1.8.
[14] SFF-TA-1027 QSFP2 Connector, Cage, and Module Specification, Rev. 1.0.
[15] SFF-TA-1031 SFP2 Cage, Connector, & Module Specification, Rev. 1.0.

9 Appendix A: Glossary

The following terms are used in this document:

Table 18: Glossary presents definitions for acronyms used in this IA

Term	Definition
CMIS	Common Management Interface Specification
CDR	Clock Data Recovery
COR	Clear on Read
DSP	Digital Signal Processing
FC	Fibre Channel
FFE	Feed forward equalizer
HW	Hardware
IA	Implementation Agreement
IntL	Interrupt on Low Transition
LSB	Least Significant Bit
LOL	Loss of Lock
LPMode	LPMode is a HW control signal that controls transition to high power mode
LS	Least Significant Bit
LSB	Least Significant Bit
MSB	Most Significant Bit
Retimer	A device that uses a recovered clock to retime the data also referred to as a CDR
RxLOS	Indicator for loss of optical signal
Rx	Receiver
RO	Read Only
RW	Read Write

Tx	Transmitter
SerDes	Serializer-Deserializer
TxDis	QSFP28/QSFP112/QSFP-DD/QSFP-DD800 hardware control to turn off transmit optics, CMIS-FF will refer to this function as TxDisable unless it is the MSA defined hardware control signal
TxDisable	Hardware or CMIS Signal that turns off transmit optics
VR	Volatile Memory
LOS	Loss of Signal

10 Appendix C: List of companies belonging to OIF when document is approved

Accelight Technologies, Inc.
Accton Technology Corporation
Adtran Networks SE
Advanced Fiber Resources (AFR)
Advanced Micro Devices, Inc.
AIO Core Co., Ltd
Alibaba
Alphawave Semi
Amazon
Amphenol Corp.
Anritsu
Applied Optoelectronics, Inc.
Arista Networks
Astera Labs
Ayar Labs
BitifEye Digital Test Solutions GmbH
BizLink Technology, Inc.
Broadcom Inc.
Cadence Design Systems
Casela Technologies USA
Celestica
China Telecom
CICT
Ciena Corporation
Cisco Systems
Coherent
ColorChip LTD
Cornelis Networks, Inc.
Corning
Credo Semiconductor (HK) LTD
Dai Nippon Printing Co., Ltd.
Dell, Inc.
Dexerials Corporation
EFFECT Photonics B.V.
Lightmatter
Linktel Technologies Co., Ltd.
Lumentum
Lumiphase AG
LUXIC Technology Co
Luxshare Technologies International, Inc.
MACOM Technology Solutions
Marvell Semiconductor, Inc.
MaxLinear Inc.
MediaTek
Meta Platforms
Microchip Technology Incorporated
Microsoft Corporation
Mitsubishi Electric US, Inc.
Molex
Multilane Inc.
NEC Corporation
Nokia
NTT Corporation
Nubis Communications, Inc.
NVIDIA
O-Net Technologies (Shenzhen) Group Co., Limited
Omniva LLC
Optomind Inc.
Orange
PETRA
Point2 Technology
Precision Optical Technologies
Quantifi Photonics USA Inc.
Quintessent Inc.
Ranovus
Retym
Rosenberger Hochfrequenztechnik GmbH & Co. KG
Samsung Electronics Co. Ltd.

Eoptolink Technology
Epson Electronics America, Inc.
Ericsson
EXFO
Foxconn Interconnect Technology Ltd
Fujikura
Fujitsu
Furukawa Electric Co., Ltd.
Global Foundries
Google
H3C Technologies Co., Ltd.
Hakusan Inc
Hewlett Packard Enterprise (HPE)
HGGenuine Optics Tech Company
Hirose Electric Co. Ltd.
Hisense Broadband Multimedia Technologies Co., LTD
Huawei Technologies Co., Ltd.
Infinera Corporation
InfiniLink
InnoLight Technology Limited
Integrated Device Technology
Intel
Juniper Networks
Kandou Bus
KDDI Research, Inc.
Keysight Technologies, Inc.
KYOCERA Corporation
Lessengers Inc.
Samtec Inc.
SCINTIL Photonics
Semtech Canada Corporation
Senko Advanced Components
SeriaLink Systems Ltd.
Sicoya GmbH
SiFotonics Technologies Inc.
Silith Technology
Socionext Inc.
Source Photonics, Inc.
Spirent Communications
Sumitomo Electric Industries, Ltd.
Sumitomo Osaka Cement
Synopsys, Inc.
TE Connectivity
Tektronix
Telefonica S.A.
TELUS Communications, Inc.
Teramount
TeraSignal, LLC.
US Conec
Viavi Solutions Deutschland GmbH
Wilder Technologies, LLC
Wistron Corporation
Xphor Ltd.
Yamaichi Electronics Ltd.
ZTE Corporation